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In re Reissue patent application of	:	
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Serial No. 09/667,643	:	Examiner L. Schillinger
Filed September 22, 2000	:	

METHOD FOR MANUFACTURING A LIQUID CRYSTAL DISPLAY

VERIFYING DECLARATION

Honorable Commissioner For Patents
Washington, D.C. 20231

Sir:

I, Young-ju Lee, declare and say:
(print name of translator)

that I am thoroughly conversant in both the Korean and English languages;

that I am presently engaged as a translator in these languages;

that the attached document represents a true English translation of the Korean Application No. **96-18516**, filed May 29, 1996.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signed this 1st day of June, 2001.

Youngjin Lee
(signature of translator)

SPECIFICATION

[Title of the Invention]

Method for Manufacturing Liquid Crystal Display

[Brief Description of the Drawings]

FIGS. 1 through 4 are sectional views illustrating a method for manufacturing a liquid crystal display according to a conventional method.

FIG. 5 is a plan view of a liquid crystal display (LCD) according to the present invention

FIGS. 6 through 11 are sectional views of a first embodiment of the manufacturing method according to the present invention.

FIG. 12 is a sectional view illustrating a TFT area of an LCD formed by a second embodiment of the manufacturing method according to the present invention.

FIG. 13 is a sectional view illustrating a gate-pad connection area of the LCD formed by the second embodiment of the manufacturing method according to the present invention.

FIG. 14 is a sectional view illustrating a gate-pad bonding area of the LCD formed by the second embodiment of the manufacturing method according to the present invention.

[Detailed Description of the Invention]

The present invention relates to a method for manufacturing a liquid crystal display (LCD), and more particularly, to a method for manufacturing an LCD through reduced number of mask processes.

A variety of plane screens or flat-panel display devices, such as a liquid crystal display (LCD) and a plasma display panel (PDP), have been replaced for conventional comparative bulky cathode-ray tubes (CRT) in order to satisfy the requests for space-

saving and personalization of display device that interfaces a computer (including other computerized machines) and a user. Among flat-panel display devices, the LCD is currently the most widely used. For a certain LCD, its color picture quality is comparable with or better than that of CRT.

The method for manufacturing a conventional LCD will be explained in detail with reference to the attached drawings.

FIGS. 1 through 4 are sectional views illustrating a conventional method for manufacturing LCD. Referring to FIGS. 1 through 4, reference characters 'A' and 'B' denote a TFT area and a gate-pad connection area, respectively.

FIG. 1 is a sectional view illustrating a step of forming a gate electrode 11 and an anode oxide film 13 on a substrate 10. After forming a metal film using aluminum (Al) on the substrate 10, a gate electrode 11 is formed by performing a first photolithography on the first metal film. Thereafter, after forming a photoresist pattern (not shown) by performing a second photolithography on a gate-pad connection area, the anode oxide film 13 is formed on the gate electrode 11 in the TFT area by anode-oxidizing the entire surface of the substrate 10. At this time, the gate-pad connection area, which is covered with the photoresist pattern, is not anode-oxidized. Then, the photoresist pattern is removed.

FIG. 2 is a sectional view illustrating a step of forming a semiconductor pattern layer on the gate electrode 11 of the TFT area. An insulating film 15 is formed on the entire surface of the substrate 10 on which the anode oxide film 13 is formed. A semiconductor film is formed by sequentially depositing an amorphous silicon film and an impurity-doped amorphous silicon film on the entire surface of the substrate 10 on which the insulating film 15 is formed. Then, a semiconductor pattern layer consisting of an amorphous silicon pattern 17 and an impurity-doped amorphous silicon pattern, is formed in the TFT area by performing a third photolithography on the semiconductor film.

FIG. 3 is a sectional view illustrating a step of forming a source electrode 21a and a drain electrode 21b in a TFT area, and a pad electrode 21c in a gate-pad

connection area at the same time. First, a contact hole is formed by performing a fourth photolithography on the insulating film 15 so that the surface of the gate electrode 11 connected to the gate-pad connection area is partially exposed. Then, the source electrode 21a and the drain electrode 21b, which are apart from the surface of the gate electrode 11, is formed in the TFT area by depositing a metal, such as Cr, on the entire surface of the substrate 10 and performing a fifth photolithography on the Cr film. The pad electrode 21c, which is connected to the gate electrode 11 through the contact hole, is formed in the gate-pad connection area. At this time, a portion of the impurity-doped amorphous silicon pattern 19 aligned with the gate electrode 11 is etched in the fifth photolithography process performed to form the source electrode 21a and the drain electrode 21b in the TFT area, so that the amorphous silicon pattern 17 formed on the gate electrode 11 is partially exposed.

FIG. 4 is a sectional view illustrating a step for forming a protective layer 23 and a pixel electrode 25 on the TFT area. First, the protective layer 23 is formed on the entire surface of the substrate 10 in the TFT area, on which the source electrode 21a and the drain electrode 21b are formed through the process described above. Next, a contact hole for a pixel electrode is formed in the drain electrode 21b by performing a sixth photolithography on the protective layer 23. At this time, the protective layer is not formed in the gate-pad connection area. Thereafter, the pixel electrode 25 is formed by depositing indium tin oxide (ITO) as a transparent electrode material and performing a seventh photolithography on the ITO. The drain electrode 21b, and the pixel electrode 25 which is formed by the seventh lithography, are connected through the contact hole for a pixel electrode that is formed by removing some portion of the protective film 23 formed on the drain electrode 21b in the sixth lithography process.

As describe above, the conventional method for manufacturing the LCD needs the first photolithography for forming the gate electrode 11, the second photolithography for forming the anode oxide film 13, the third photolithography for forming the semiconductor pattern layer, the fourth photolithography for forming the contact hole, the fifth photolithography for forming the source electrode 21a, the drain electrode 21b,

and the pad electrode 21c, the sixth photolithography for forming the contact hole for a pixel electrode, and the seventh photolithography for forming the pixel electrode 25. Therefore, both manufacturing time and cost increase and the yield becomes lower.

In order to reduce the number of the photolithography processes, in a conventional method, a refractory metal film having a high resistance has been adopted as a gate electrode while omitting the anode-oxidizing process. However, this causes distortion of a gate signal to occur when it is applied to manufacture a large-sized LCD which is greater than 10 inches, and in turn a driving problem. Further, if a gate-pad connection area is formed of ITO and aluminum, indium (In) diffuses into aluminum at high-temperature processes, so that there is a problem in that contact resistance increases.

To solve the above problems, it is an object of the present invention to provide a more efficient method of manufacturing a liquid crystal display in which a contact resistance in a gate-pad connection area becomes low and the number of the photography processes is reduced by omitting photolithography processes for forming an anode oxide film and a contact hole.

To achieve the above object of the present invention, in one embodiment, there is provided a method for manufacturing a LCD having a TFT area and a gate-pad connection area , comprising the steps of: (a) forming a gate electrode by depositing a first metal film and a second metal film on the entire surface of a substrate and performing a first photolithography on the second metal film and the first metal film; (b) forming a semiconductor pattern layer to be used as an active region in the TFT area by forming an insulating film and a semiconductor film on the entire surface of the substrate on which the gate electrode is formed, and by performing a second photolithography on the semiconductor film; (c) forming a source electrode and a drain electrode in the TFT area, and a pad electrode in the gate-pad connection area, by forming a third metal film on the entire surface of the substrate having the semiconductor pattern layer and by performing a third photolithography on the third metal film and the semiconductor pattern layer; (d) forming a protective film on the

entire surface of the substrate on which the source electrode, the drain electrode and the pad electrode are formed, and forming a protective pattern by performing a fourth photolithography process on the protective film and the insulating film, through which the drain electrode in the TFT area and the gate electrode and pad electrode in the gate-pad connection area are exposed; (e) forming a pixel electrode which is connected to the drain electrode and by which the pad electrode and the gate electrode are connected, by etching the second metal film using the protective pattern as an etching mask, exposing the surface of the first metal film in the gate-pad connection area, and depositing a fourth metal film for a pixel electrode.

It is preferable that, in step (a), the first metal film is formed by depositing a refractory metal such as Cr, Ta, Mo and Ti to a thickness between 300Å and 4000Å and the second metal film is formed by depositing Al or Al alloy to a thickness between 1000Å and 4000Å. It is preferable that, in the first photolithography process of step (a), taper etching is performed on the second metal film and the first metal film is consecutively etched. Thus, in the gate electrode, the first metal film is formed to be wider than the second metal film. The LCD manufacturing method may further comprises a step of performing an anode oxidization after forming the gate electrode.

It is preferable that, in step (b), the insulating film is formed of SiNx to have a thickness between 2000Å and 9000Å. The semiconductor film may be formed as a double film by consecutively depositing amorphous silicon (a-Si) and impurity-doped amorphous silicon (n^+ a-Si).

It is preferable that, in step (c), the third metal film is deposited using Cr or Ti to have a thickness between 300Å and 4000Å. It is preferable that, in step (d), the protective film is formed of SiNx.

It is preferable that, in step (e), the fourth metal film for a pixel electrode is formed of indium-tin oxide (ITO).

In another embodiment of the present invention, there is provided a method for manufacturing a liquid crystal display having a TFT area, a gate-pad connection area, and a gate-pad bonding area, comprising the steps of: (a) forming a gate electrode and

a gate pad pattern by sequentially depositing a first metal film and a second metal film on the entire surface of a substrate and performing a first photolithography on the second metal film and the first metal film; (b) forming a semiconductor pattern layer, which is used as an active region in the TFT area, by forming an insulating film and a semiconductor film on the entire surface of the substrate having the gate electrode and the gate pad pattern and by performing a second photolithography on the semiconductor film; (c) forming a source/drain electrode and a source/drain pad pattern in the TFT area by forming a third metal film on the entire surface having the semiconductor pattern layer, and performing a third photolithography on the third metal film and the semiconductor pattern layer; (d) forming a protective film on the entire surface of the substrate on which the source electrode, drain electrode, and pad electrode are formed, and forming a protective pattern by performing a fourth photolithography process on the protective film and the insulating film, through which the drain electrode in the TFT area and the gate electrode and gate pad pattern in the gate-pad connection area are exposed; (e) forming a pixel electrode which is connected to the drain electrode and by which the pad electrode and the gate electrode are connected, by performing a fifth photolithography process on the second metal film using the protective pattern as an etching mask, exposing the surface of the first metal film in the gate-pad connection area, and depositing a fourth metal film for a pixel electrode.

It is preferable that, in step (a), the first metal film is formed by depositing a refractory metal such Cr, Ta or Ti to have a thickness between 300Å and 4000Å, and the second metal film is formed by depositing Al or Al alloy to have a thickness between 1000Å and 4000Å. The gate electrode pattern and the pad electrode pattern are preferably formed at the same time. It is preferable that, in the first photolithography process, taper etching is performed on the second metal film and the first metal film is consecutively etched.

It is preferable that, in step (b), the insulating film is formed as a single film of Sinx or a double film of Sinx and SiOx to have a thickness 2000Å and 9000Å. The

semiconductor film may be formed by sequentially depositing amorphous silicon (a-Si) and impurity-doped amorphous silicon (n^+ a-Si).

It is preferable that, in step (c), the third metal film is formed by depositing Cr, Ti or Mo to have a thickness between 300Å and 4000Å. In step (d), the protective film may be formed of SiNx. The fourth metal film for a pixel electrode may be formed of indium-tin oxide (ITO) in step (e).

As described above, the present invention has advantages in that a large-sized LCD can be manufactured at low cost through five photolithography processes, which is less than those conducted in the conventional method.

Hereafter, the preferable embodiments of the method for manufacturing a LCD according to the present invention will be described in greater detail with reference to the attached drawings.

Embodiment 1

FIG. 5 is a plan view of a LCD according to the present invention.

Referring to FIG. 5, a gate line (gate: 1) is formed in the horizontal direction and a gate pad (3) connected to the gate line (1) is formed. A thin film transistor (5) and a pixel electrode (7) are connected to the gate line (1). Further, a data line (8) is formed in the vertical direction and a data pad (9) connected to the data line (8) is formed.

FIGS. 6 through 11 are sectional views illustrating a first embodiment of the LCD manufacturing method according to the present invention. Refering to FIGS. 6 through 11, reference characters C and D denote a TFT area and a gate-pad connection area, respectively.

In FIG. 6, a first metal film (31) is formed of Cr on a substrate (30) to have a thickness between 300Å and 4000Å. Thereafter, a second metal film (33) is formed of Al alloy on the first metal film (31) to have a thickness between 1000Å and 4000Å. The first and second metal films (31, 33) can be formed consecutively. A gate electrode is then formed by performing a first photolithography on the first and second metal films (31, 33). In the first photolithography process, taper etching is performed

on the second metal film and the second metal film is etched, so that the first metal film (31) is formed to be wider than the second metal film (33).

In FIG. 7, an insulating film (35) is formed of a nitride film or an oxide film on the entire surface of the substrate (30), and a semiconductor film consisting of an amorphous silicon film (37) and an impurity-doped amorphous silicon film (39) is formed on the entire surface of the substrate (30) on which the insulating film (35) is formed. The insulating film (35) is formed to have a thickness between 2000Å and 9000Å. The amorphous silicon film (37) is formed to have a thickness between 1000Å and 4000Å and the impurity-doped amorphous silicon film (39) is formed to have a thickness between 300Å and 1000Å, respectively. Then a semiconductor pattern layer as double layers including the amorphous silicon film (37) and the impurity-doped amorphous silicon film (39) is formed in the TFT area by performing a second photolithography on the semiconductor film.

In FIG. 8, a third metal film is formed of Cr or Ti to have a thickness between 300Å and 4000Å on the substrate (30) in which the semiconductor pattern layer and the insulating film (35) are formed. Then a source electrode (41b) and a drain electrode (41c) are formed in the TFT area and a pad electrode (41a) is formed in the gate-pad connection area, by performing a third photolithography on the third metal film. At this time, the impurity-doped amorphous silicon film in the TFT area is etched and therefore, the amorphous silicon film (37) is exposed.

In FIG. 9, a protective pattern (43) is formed on the entire surface of the substrate (30) by forming a protective film with a nitride film or the like and performing a fourth photolithography on the protective film. At this time, a portion of the protective film on the drain electrode (41c) in the TFT area is etched thereby exposing a portion of the drain electrode (41c). The insulating film (35) on the gate electrode in the gate-pad connection area, i.e., on the second metal film (33), is etched thereby exposing the surface of the gate electrode. A portion of the protective film on the pad electrode (41a) is also etched.

In FIG. 10, the second metal film (33), which is positioned in the gate electrode-

pad connection area and indicated as reference numeral '45' and is exposed through the protective pattern (43), is etched. As a result, contact resistance between the second metal film (33) and a pixel electrode to be formed in a subsequent process can be reduced.

In FIG. 11, a pixel electrode (47) is formed by depositing indium-tin oxide (ITO) as a transparent electrode material on the entire surface of the substrate (30) having the protective film pattern and by performing a fifth photolithography on the ITO. As a result, the drain electrode (41c) and the pixel electrode (47) are connected in the TFT area, and the gate electrode consisting of the first and second metal films (31, 33), and the pad electrode (41a) are connected by the pad electrode 41a in the gate-pad connection area.

Embodiment 2

FIGS. 12 through 14 are sectional views illustrating an LCD formed by the method according to the second embodiment of the present invention. Specifically, FIGS. 12, 13 and 14 show a TFT area, a gate-pad connection area, and a gate pad bonding area, respectively.

The second embodiment of the LCD manufacturing method according to the present invention will be described in greater detail with reference to FIGS. 12 through 14.

A first metal film (51) is formed by depositing a refractory metal such as Cr, Ta or Ti on a substrate (50) to have a thickness between 300Å and 4000Å. Next, a second metal film (53) is formed by depositing Al or Al alloy on the first metal film (51) to have a thickness between 1000Å and 4000Å. The second metal film 53 and the first metal film 51 are sequentially etched by a first photolithography process to form a gate electrode and gate pad patterns. A pad electrode pattern is formed at the same time as the gate electrode pattern. In the first photolithography process, taper etching is performed on the second metal film 53 and the first metal film 51 is consecutively etched. As a result, the first metal film (51) become wider than the second metal film

(53).

Next, an insulating film (55) and a semiconductor film are formed on the entire surface of the substrate 50 on which the gate electrode and the gate pad pattern are formed. A semiconductor pattern layer (57) to be used as an active area is formed in the TFT area by performing a second photolithography on the semiconductor film. At this time, the insulating film (55) is formed as a single film of SiNx or a double film of SiNx and SiOx to have a thickness between 2000Å and 9000Å. The semiconductor pattern layer (57) is formed by continuously depositing amorphous silicon (a-Si) and impurity-doped amorphous silicon (n^+ a-Si).

Thereafter, a third metal film is formed by depositing Cr, Ti, or Mo to have a thickness between 300Å and 4000Å on the entire surface of the substrate (50) on which the semiconductor pattern layer (57) is formed, and a source/drain electrode (61) is formed in the TFT area by performing a third photolithography on the third metal film (61) and the semiconductor pattern layer (57).

Then, a protective film (61) is formed of SiNx on the entire surface of the substrate (50) and a contact hole through which a portion of the drain electrode placed in the TFT area is exposed is formed by performing a fourth photolithography on the protective film (63).

Then, a pixel electrode, which is connected to the drain electrode, is formed by depositing a fourth metal film (67) for a pixel electrode using ITO.

As descrinbed above, the method for manufacturing a liquid crystal display according to the present invention can form double gate electrodes through five or six lithography processes, so that the manufacturing cost can be remarkably reduced and the manufacturing yield can be improved, compared to the conventional method in which seven photolithography processes are applied.

Also, it is possible to suppress the growth of a hillock of the Al film due to stress relaxation effect of the chromium and Al films formed as double gate electrodes.

As shown in FIG. 10, it is possible to reduce the contact resistance between the Al film of the gate electrode and the pixel electrode to be formed in a subsequent

process by etching the Al film in the gate-pad connection area, prior to forming the gate electrode.

While this invention has been particularly shown and described with reference to preferred embodiments thereof The present invention is not restricted to the above embodiments, and it is clearly understood that many variations can be possible within the scope and spirit of the present invention by any one skilled in the art.

What is claimed is:

1. A method for manufacturing a liquid crystal display having a TFT area and a gate-pad connection area, comprising the steps of:

(a) forming a gate electrode by depositing a first metal film and a second metal film on the entire surface of a substrate and performing a first photolithography on the second metal film and the first metal film;

(b) forming a semiconductor pattern layer to be used as an active region in the TFT area by forming an insulating film and a semiconductor film on the entire surface of the substrate on which the gate electrode is formed, and by performing a second photolithography on the semiconductor film;

(c) forming a source electrode and a drain electrode in the TFT area, and a pad electrode in the gate-pad connection area, by forming a third metal film on the entire surface of the substrate having the semiconductor pattern layer and by performing a third photolithography on the third metal film and the semiconductor pattern layer;

(d) forming a protective film on the entire surface of the substrate on which the source electrode, the drain electrode and the pad electrode are formed, and forming a protective pattern by performing a fourth photolithography process on the protective film and the insulating film, through which the drain electrode in the TFT area and the gate electrode and pad electrode in the gate-pad connection area are exposed;

(e) forming a pixel electrode which is connected to the drain electrode and by which the pad electrode and the gate electrode are connected by etching the second metal film using the protective pattern as an etching mask, exposing the surface of the first metal film in the gate-pad connection area, and depositing a fourth metal film for a pixel electrode.

2. The method as claimed in claim 1, wherein, in step (a), the first metal film is formed of a refractory metal and the second metal film is formed of Al or Al alloy.

3. The method as claimed in claim 2, wherein the refractory metal is one

selected from the group consisting of Cr, Ta and Ti.

4. The method as claimed in claim 2, wherein the first metal film is deposited to have a thickness between 300Å and 4000Å and the second metal film is deposited to have a thickness between 1000Å and 4000Å.

5. The method as claimed in claim 1, wherein, in the first photolithography process of step (a), taper etching is performed on the second metal film and the first metal film is consecutively etched.

6. The method as claimed in claim 1, wherein the first metal film is formed to be wider than the second metal film.

7. The method as claimed in claim 1, further comprising a step of performing anode oxidation immediately after forming the gate electrode.

8. The method as claimed in claim 1, wherein the insulating film is formed of SiNx in the step (b).

9. The method as claimed in clam 8, wherein the insulating film is formed to have a thickness between 2000Å and 9000Å.

10. The method as claimed in claim 1, wherein, in step (b), the semiconductor film is formed as double films by continuously depositing amorphous silicon (a-Si) and impurity-doped amorphous silicon (n^+ a-Si).

11. The method as claimed in claim 1, wherein, in step (c), the third metal film is formed of Cr or Ti.

12. The method as claimed in claim 11, wherein the third metal film is deposited to have a thickness between 300Å and 4000Å.

13. The method as claimed in claim 1, wherein the protective film is formed of SiNx in step (d).

14. The method as claimed in claim 1, wherein the fourth metal film for a pixel electrode is formed of indium-tin oxide (ITO) in step (e).

15. A method for manufacturing a liquid crystal display having a TFT area, a gate-pad connection area, and a gate-pad bonding area, comprising the steps of:

(a) forming a gate electrode and a gate pad pattern by sequentially depositing a first metal film and a second metal film on the entire surface of a substrate and performing a first photolithography on the second metal film and the first metal film;

(b) forming a semiconductor pattern layer, which is used as an active region in the TFT area, by forming an insulating film and a semiconductor film on the entire surface of the substrate having the gate electrode and the gate pad pattern and by performing a second photolithography on the semiconductor film;

(c) forming a source/drain electrode and a source/drain pad pattern in the TFT area by forming a third metal film on the entire surface having the semiconductor pattern layer, and performing a third photolithography on the third metal film and the semiconductor pattern layer;

(d) forming a protective film on the entire surface of the substrate on which the source electrode, drain electrode, and pad electrode are formed, and forming a protective pattern by performing a fourth photolithography process on the protective film and the insulating film, through which the drain electrode in the TFT area and the gate electrode and gate pad pattern in the gate-pad connection area are exposed;

(e) forming a pixel electrode which is connected to the drain electrode and by which the pad electrode and the gate electrode are connected, by performing a fifth

photolithography process on the second metal film using the protective pattern as an etching mask, exposing the surface of the first metal film in the gate-pad connection area, and depositing a fourth metal film for a pixel electrode.

16. The method as claimed in claim 15, wherein the first metal film is formed of a refractory metal and the second metal film is formed of Al or Al alloy in step (a).

17. The method as claimed in claim 16, wherein the refractory metal is one selected from the group consisting of Cr, Ta and Ti.

18. The method as claimed in claim 16, wherein the first metal film is formed to have a thickness between 300Å and 4000Å and the second film is formed to have a thickness between 1000Å and 4000Å.

19. The method as claimed in claim 15, wherein the gate electrode pattern and the pad electrode pattern are simultaneously formed in step (a).

20. The method as claimed in claim 15, wherein, in the first photolithography process of step (a), taper etching is performed on the second metal film and the first metal film is consecutively etched..

21. The method as claimed in claim 15, wherein the insulating film is formed of SiNx in step (b).

22. The method as claimed in claim 21, wherein the insulating film is formed to have a thickness between 2000Å and 9000Å.

23. The method as claimed in claim 1, wherein the insulating film is formed

as double films by sequentially depositing SiNx and SiOx in step (b).

24. The method as claimed in claim 15, wherein the semiconductor film is formed by continuously depositing amorphous silicon (a-Si) and impurity-doped amorphous silicon (n+ a-Si) in step (b).

25. The method as claimed in claim 15, wherein the third metal film is formed of one selected from the group consisting of Cr, Ti and Mo in step (c).

26. The method as claimed in claim 25, wherein the third metal film is deposited to have a thickness between 300Å and 4000Å.

27. The method as claimed in claim 15, wherein the protective film is formed of SiNx in step (d).

28. The method as claimed in claim 15, wherein the fourth metal film for a pixel electrode is formed of indium-tin oxide (ITO) in step (e).

ABSTRACT

A method for manufacturing a liquid crystal display through reduced number of mask processes is provided. In the method for manufacturing an LCD having a TFT area and a gate-pad connect area, a gate electrode is formed as double layers including a first metal film and a second metal film, and a second metal film located in the gate-pad connect area is etched so that the first metal film and a pad electrode are connected by a pixel electrode. Therefore, it is possible to manufacture a large-sized LCD through reduced number of photolithography processes, e.g., through five photolithography processes, at low cost.

[Representative Drawings]

FIGS. 8 through 11

FIG. 1

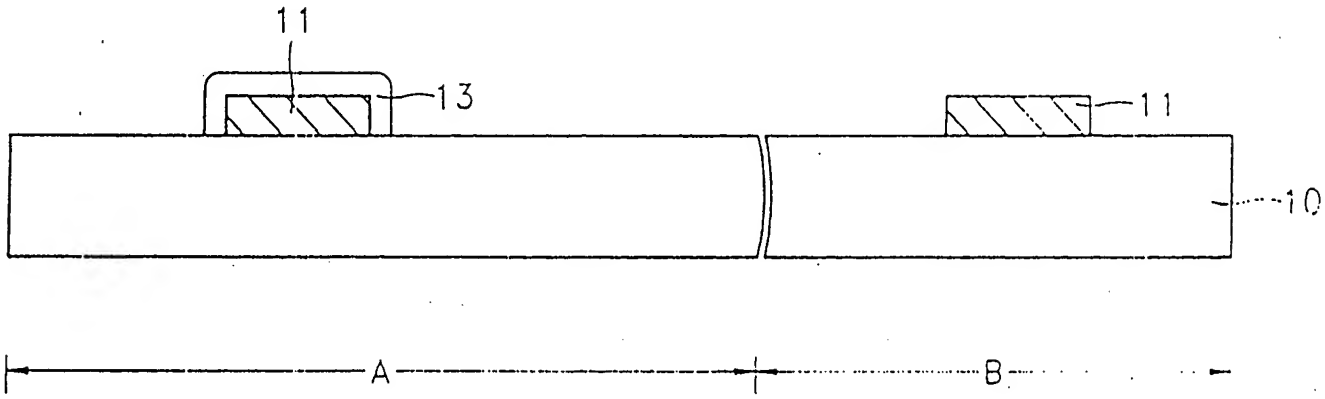

FIG. 2

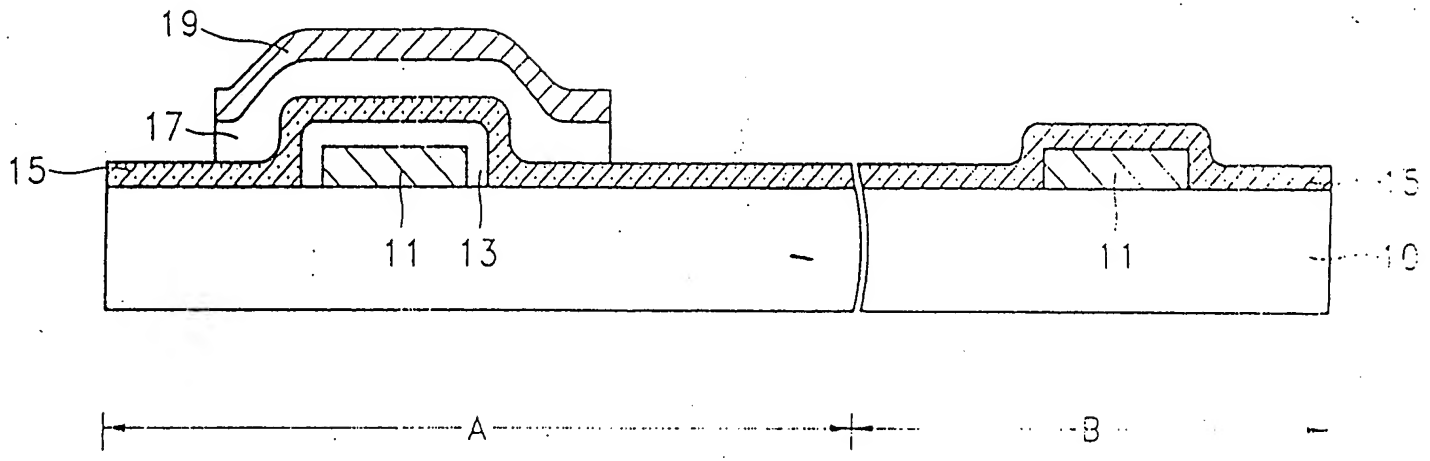

FIG. 3

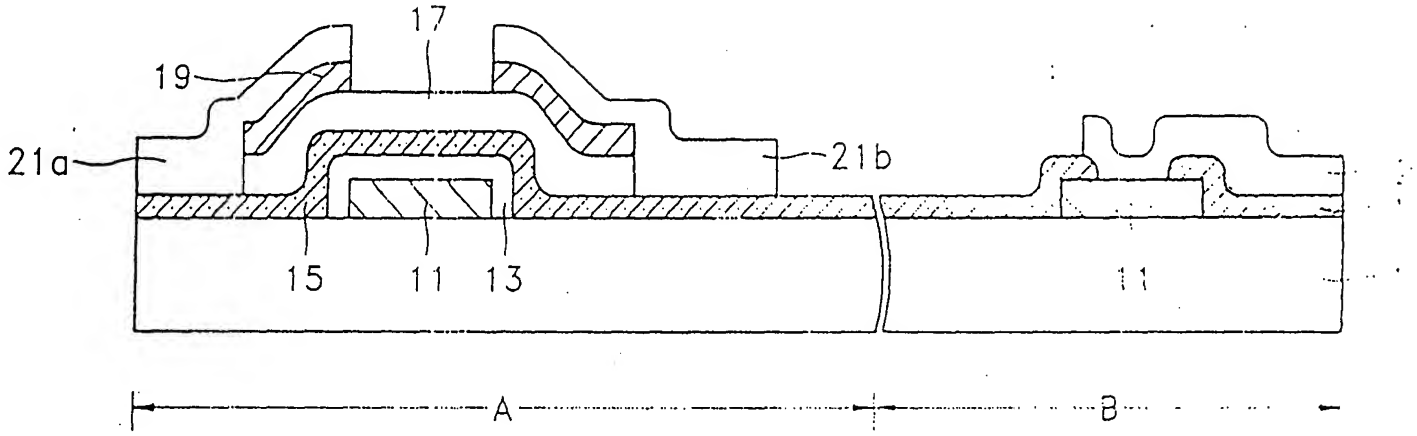

FIG. 4

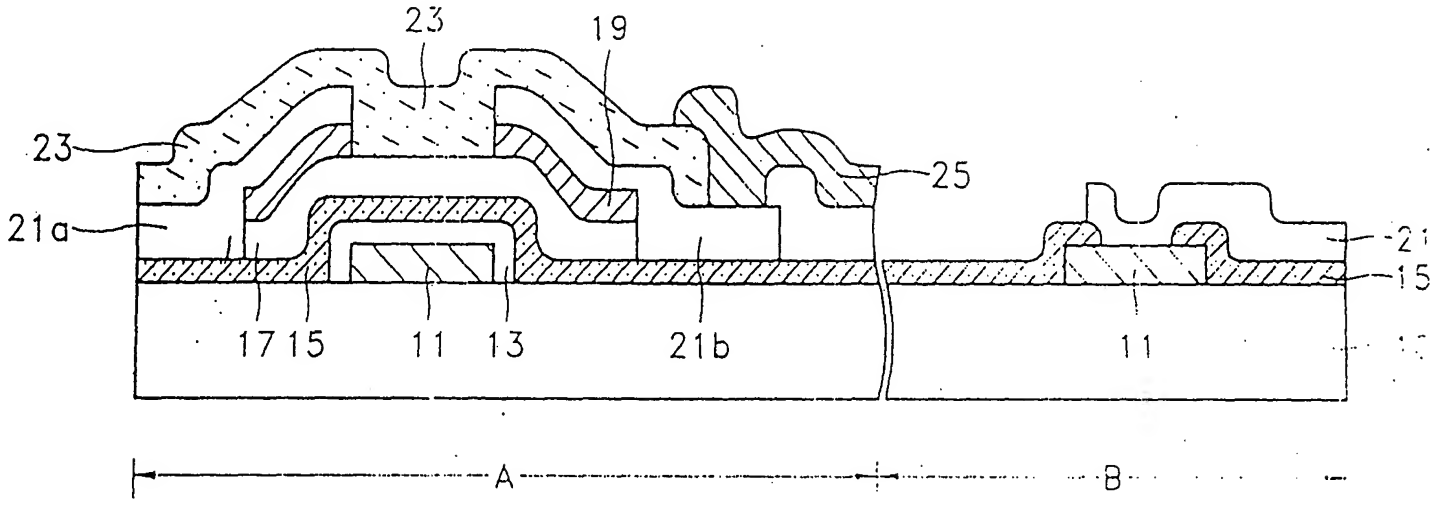

FIG. 5

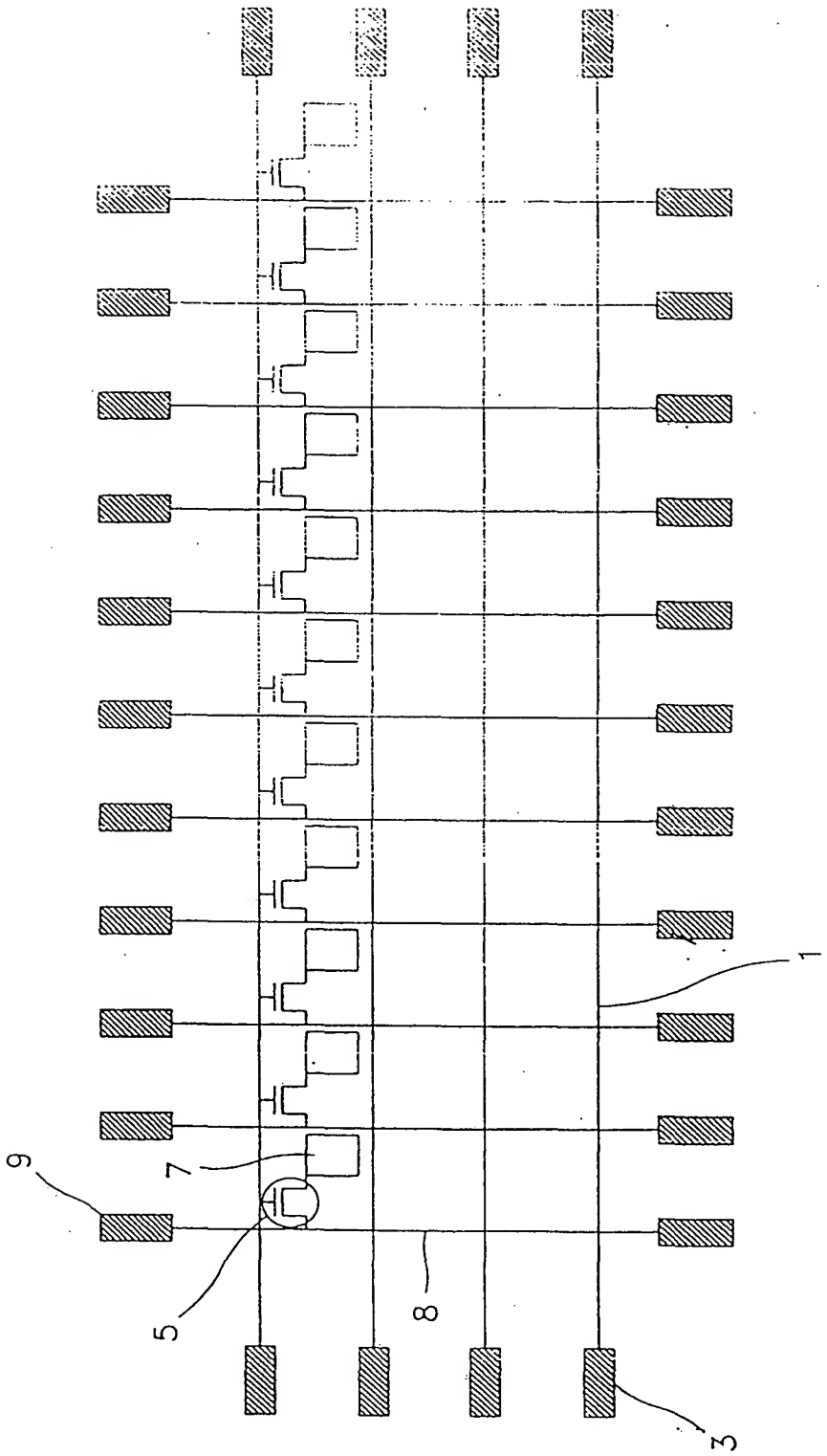

FIG. 6

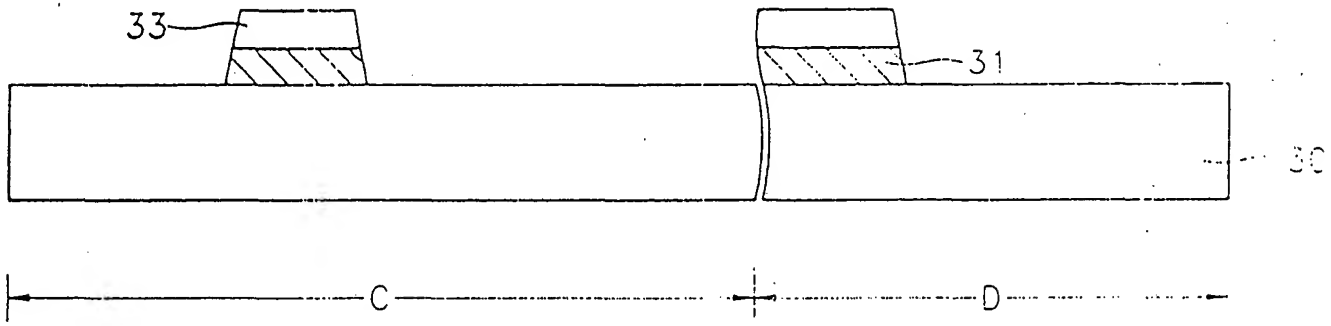

FIG. 7

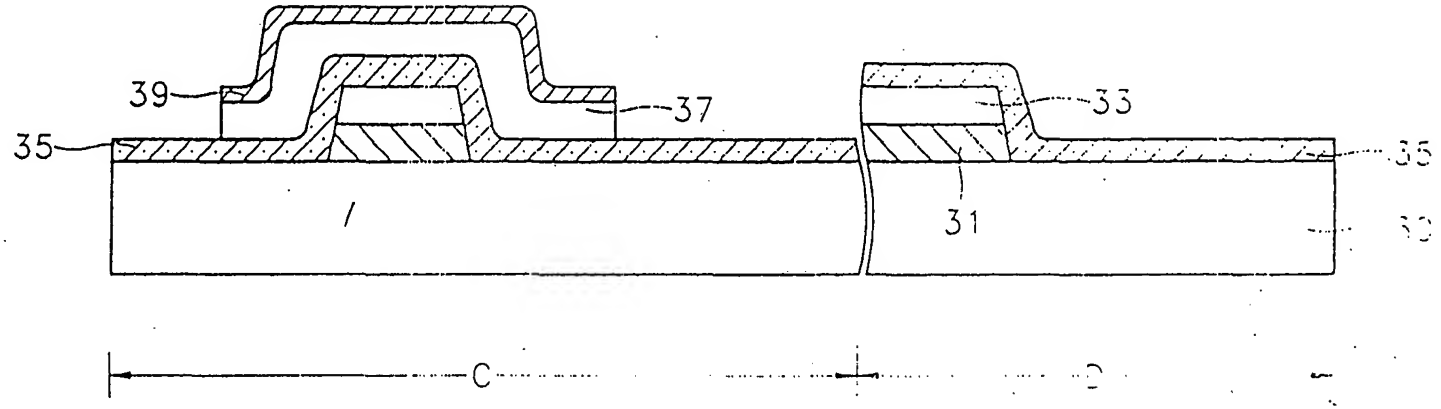

FIG. 8

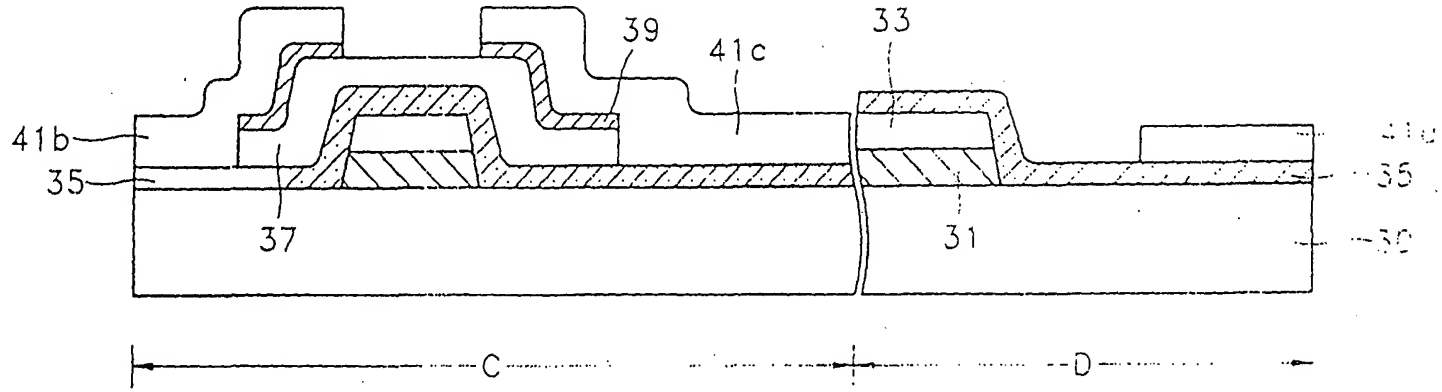

FIG. 9

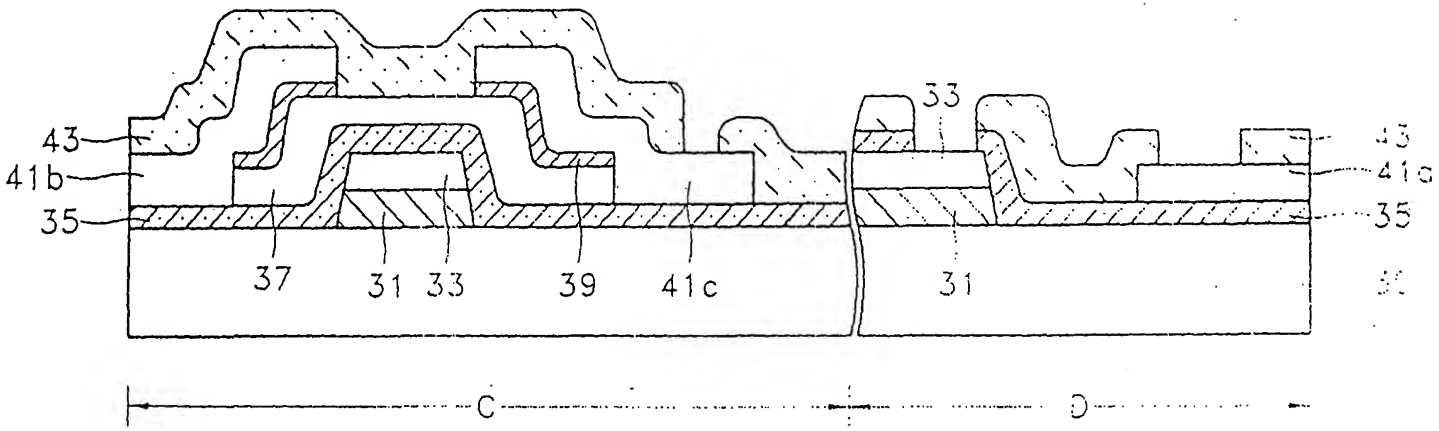

FIG. 10

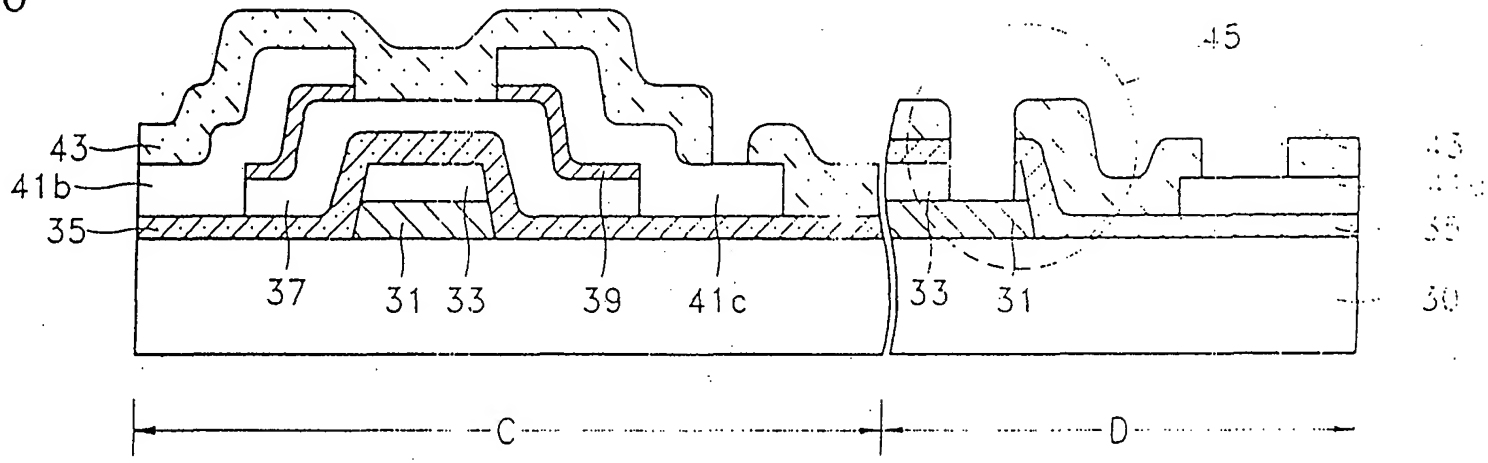
45
43
41b
35
37
31
33
39
41c
33
31
C
D

FIG. 11

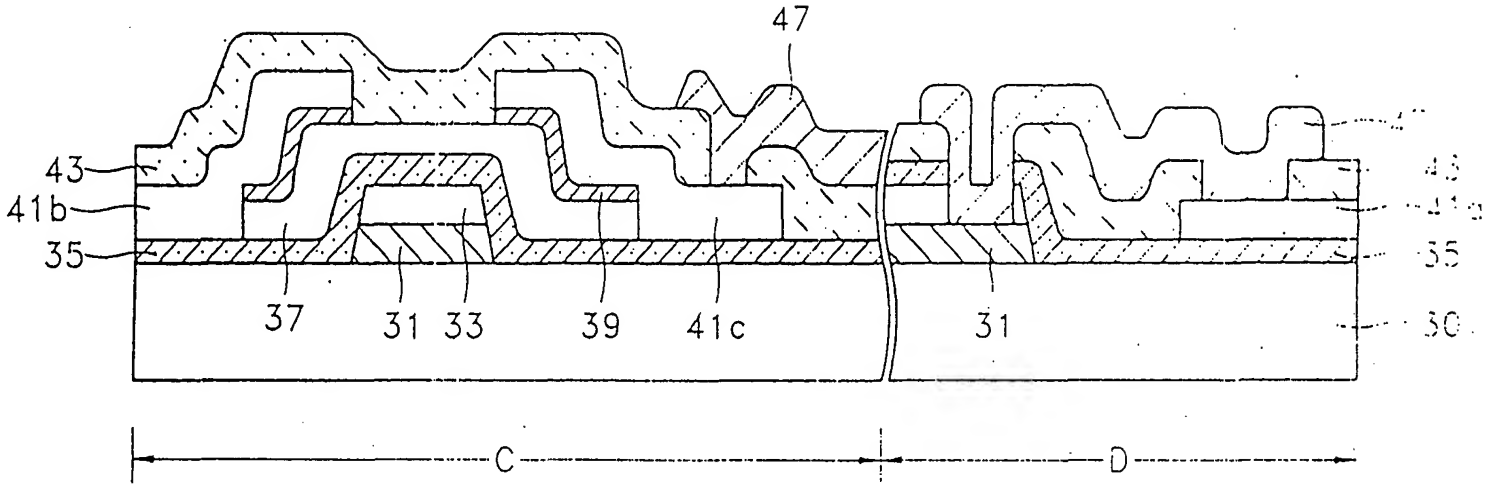
47
43
41b
35
37
31
33
39
41c
31
C
D

FIG. 12

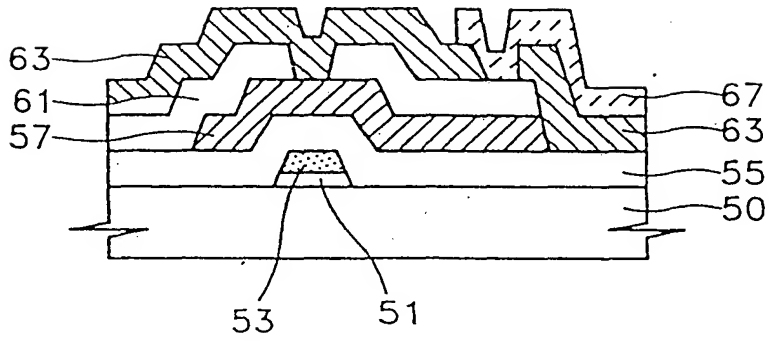

FIG. 13

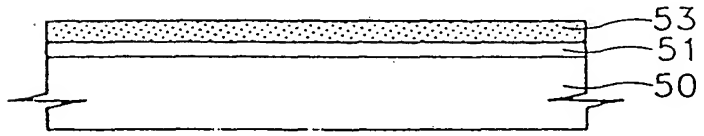

FIG. 14